Attorney's Docket No.: 10559-515001 / P12419

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Eidson et al. Art Unit: 2183
Serial No.: 09/994,483 Examiner: Kevin P. Rizzuto
Filed: November 26, 2001
Title: SYSTEM-ON-CHIP BREAKPOINT SYNCHRONIZATION

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Pursuant to United States Patent and Trademark Office OG Notices: 12 July 2005 - New Pre-Appeal Brief Conference Pilot Program, a request for a review of an initial matter is hereby submitted with the Notice of Appeal. Review of this matter by a panel of examiners is requested because the rejections are clearly not proper and are without basis, in view of a clear legal or factual deficiency in the rejections. The right to address additional matters, including but not limited to the proper interpretation of claim terminology, in any subsequent appeal brief are reserved.

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In the action mailed August 4, 2005, claims 1-27, 29-30, 32-33, 35-36, 38-40, and 42 were rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 4,502,116 to Fowler et al. (hereinafter "Fowler") and U.S. Patent No. 5,956,514 to Wen et al. (hereinafter "Wen").

Applicants traverse these rejections. However, for the sake of limiting issues before the panel, Applicants requests that the panel review be limited to the following issue:

1. Does the combination of Fowler and Wen support a *prima facie* case of obviousness of claims 1, 7, 15, 17, and 23?

Independent claim 1, which is illustrative, relates to continuing execution of a breakpoint by a processor in response to receipt of a signal indicating that the state of a peripheral has been saved.

The rejection is based on the contention that processors in a multiprocessor system are "peripherals." Although Applicant vehemently disagrees, even if processors in a multiprocessor system were peripherals, Fowler and Wen still fail to describe or suggest elements and/or limitations in claim 1 and a *prima facie* case of obviousness has not been established.

In particular, Fowler and Wen fail to describe or suggest continuing execution of a breakpoint in response to receipt of a signal indicating that the state of a peripheral has been saved, as recited in claims 1, 7, 15, 17, and 23.

In this regard, Fowler specifies that his interface circuit handles four different types of signals, i.e., pause-in signals, pause-out signals, resume-in signals, and resume-out signals. None of these signals indicates anything about the save state of another processor. Fowler thus teaches that any instruction execution is independent of the save state of other processors in his multiprocessor system. This stands in direct contrast to claims 1, 7, 15, 17, and 23, in which execution of a breakpoint is continued in response to receipt of a signal indicating that the state of a peripheral has been saved.

Even if one of ordinary skill were to ignore this teaching of Fowler that there is no need for information about the save state of processors and to add Wen's breakpoint exception handler to Fowler's system, the combination would not continue execution of a breakpoint in response to receipt of a signal indicating that the state of a peripheral has been saved in the combined system, as recited in claims 1, 7, 15, 17, and 23.

In this regard, Wen describes that a breakpoint exception handler CSU 80 can be executed on the *slave processors* of his multiprocessor system. *See Wen*, col. 7, line 36-37. When one such slave processor reaches a breakpoint, the breakpoint exception handler at that slave processor saves the local register contents of the application program, sends a command to a master processor to *stop execution* of other processors, and the slave exits the application program and jumps to the monitor software command loop 72. *See Wen*, col. 7, line 36-41 (describing the sequence of steps undertaken by the slave

processor); *Wen*, col. 7, line 30-34, col. 6, line 42-45, and col. 6, line 19-32 (providing additional detail regarding the distinctions between application run-time and monitor modes in Wen's system). This slave thus initiates a system-wide stop to the execution of application programs and entry into monitoring loops with a signal generated after the slave's state has been saved.

Once Wen's initiating slave processor *exits* application run-time, no subsequent execution of the breakpoint by the initiating slave is described in Wen's disclosure. In other words, there is no indication that Wen's slave does anything other than *stopping* processing of the application and entering into the monitor software mode. There is therefore no description in Wen of any kind that the breakpoint is subsequently executed by the initiating slave or otherwise, much less that other processors somehow signal their save state to the initiating slave and that subsequent execution responds to these signals from other processors.

Indeed, the only response made by any processor in Wen's system to the signal generated after the initiating slave has saved its state is to stop execution. Applicant respectfully submits that stopping execution of an application in response to a signal generated after a state of a processor has been saved neither describes nor suggests continuing execution of a breakpoint in response to receipt of a signal indicating that the state of a peripheral has been saved. Indeed, Wen is teaching nearly the opposite of what Applicant is claiming.

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Thus, a clear factual basis for why a *prima facie* case of obviousness of claims 1, 7, 15, 17, and 23 has not been established has been set forth and this issue is ripe for panel review. Further, in light of this basis, claims 1, 7, 15, 17, 23, and the claims dependent therefrom are patentable over Wen and Fowler in any combination.

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Respectfully submitted,

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